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Digital Systems Design Project 1

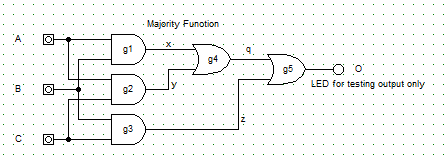
10-27-16

**3-Input Majority Function**

Our majority function will take 3 inputs and will return 1 or 0 based on which input there is the most of. For example, if there are two 1s passed and one 0 then the function will return 1, and if two 0s are passed and one 1 then the function will return 0. This makes the name of the function descriptive, as the name of the function describes that it returns the value for which a majority are input. This function was implemented with three AND gates and two OR gates.

|  |  |  |  |
| --- | --- | --- | --- |
| **3-Input Majority Function Truth Table** | | | |
| **A** | **B** | **C** | **O** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **3-Input Majority Function Map** | | | | | |
| **X** | **YZ** | | | | |
|  | **00** | **01** | **11** | **10** |
| **0** |  |  | 1 |  |
| **1** |  | 1 | 1 | 1 |



module majority(A,B,C,O);

input A,B,C;

output O;

wire x,y,z,q;

and g1 (x,A,B),

g2 (y,A,C),

g3 (z,B,C);

or g4 (q,x,y),

g5 (O,q,z);

endmodule

module test;

reg A,B,C; // Reg for inputs

wire O; // Wire for outputs

majority M(A,B,C,O);

initial

begin

$display("Time A B C O");

A=0; B=0; C=0;

#10 A=0; B=0; C=1;

#10 A=0; B=1; C=0;

#10 A=0; B=1; C=1;

#10 A=1; B=0; C=0;

#10 A=1; B=0; C=1;

#10 A=1; B=1; C=0;

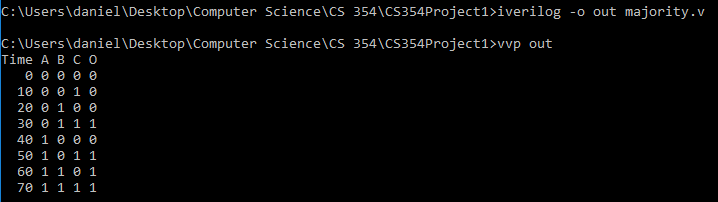
#10 A=1; B=1; C=1;

end

initial

$monitor("%4d %b %b %b %b",$time,A,B,C,O);

endmodule



**Conditional Inverter (without XOR)**

The point of a conditional inverter is to have a mode input and a value input.

